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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	RICHARD W. FOOTE ET AL.
U.S. Serial No.	:	10/777,012
Filed	:	February 11, 2004
For	:	SEMICONDUCTOR APPARATUS COMPRISING BIPOLAR TRANSISTORS AND METAL OXIDE SEMICONDUCTOR TRANSISTORS AND MANUFACTURING METHOD
Group No.	:	2891
Examiner	:	Steven J. Fulk

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

This Appeal Brief Under 37 C.F.R. § 41.37 ("Appeal Brief") is in furtherance of the Notice of Appeal filed in this application on April 10, 2007 that was received by the Patent and Trademark Office on April 13, 2007. The date for filing this Appeal Brief is June 13, 2007.

Real Party in Interest **37 C.F.R. § 41.37 (c)(1)(i)**

This patent application is currently owned by National Semiconductor Corporation, a corporation having a place of business at 2900 Semiconductor Drive, Santa Clara, California, 95051, as evidenced by an Assignment from the inventors Richard W. Foote and Robert Oliver. The Assignment was recorded in the Patent and Trademark Office on February 11, 2004 on Reel 014979 and Frame 0973.

Related Appeals or Interferences **37 C.F.R. § 41.37 (c)(1)(ii)**

None. There are no appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

Status of Claims **37 C.F.R. § 41.37 (c)(1)(iii)**

Claims 1-4, 7-10, 13-17, 20 and 21 have been rejected in a final Office Action dated January 10, 2007.

Claims 1-4, 7-10, 13-17, 20 and 21 are presented for appeal.

Claims 22-42 have been previously withdrawn.

Claims 5-6, 11-12 and 18-19 have been cancelled.

A copy of the claims involved in the appeal is provided in Appendix A.

Status of Amendments after Final **37 C.F.R. § 41.37 (c)(1)(iv)**

No amendments to the claims have been submitted and refused entry after issuance of the final Office Action dated January 10, 2007.

Summary of Claimed Subject Matter **37 C.F.R. § 41.37 (c)(1)(v)**

The following general discussion provides background for understanding the invention. A concise explanation of the subject matter of the invention defined in each of the independent claims involved in the appeal is set forth below after the general discussion.

General Discussion

The present invention provides a semiconductor apparatus that comprises a double poly bipolar transistor and a double poly metal oxide semiconductor (MOS) transistor in which (1) a base of the double poly bipolar transistor and (2) a gate of the double poly metal oxide semiconductor (MOS) transistor contain substantially identical dopants.

The transistors of the semiconductor apparatus of the invention comprise a PNP bipolar transistor device, an NPN bipolar transistor device, a PMOS transistor device and an NMOS transistor device. The transistor devices are manufactured in a unified process in which a first polysilicon layer 2700 (Poly1 2700) is doped to form an extrinsic base 2810 in the PNP device and an NMOS gate 2820 in the NMOS device. (Specification, Page 29, Paragraph [00112], Figure 28). The first polysilicon layer 2700 (Poly 1 2700) is then doped to form an extrinsic base 2910 in the NPN device and a PMOS gate 2920 in the PMOS device. (Specification, Page 30, Paragraph [00114], Figure 29). The respective bases and gates each receive the same dopant because they are simultaneously doped with the same dopant process.

An Inter Poly Dielectric (IPD) layer 3000 is then deposited. A mask and etch procedure is then applied to etch through portions of the IPD layer 3000 and through the doped extrinsic base

2810 in the PNP device (to form extrinsic base portions 3140 and 3150) and through the doped extrinsic base 2910 in the NPN device (to form extrinsic base portions 3120 and 3130). (Specification, Pages 30-33, Paragraphs [00116] to [00120], Figures 30-31). A mask and etch procedure is then applied to etch through portions of the IPD layer 3000 and through portions of the doped polysilicon layer 2820 in the NMOS device (to form NMOS gate 2820) and through portions of the doped polysilicon layer 2920 in the PMOS device (to form PMOS gate 2920). (Specification, Pages 33-34, Paragraphs [00121] to [00124], Figure 32).

Implant procedures are used to dope the intrinsic bases of the bipolar transistors and to dope the Lightly Doped Drains (LDD) of the MOS transistors. Specifically, an implant procedure is used to dope the intrinsic base 3410 of the NPN device and the LDDs 3420 and 3430 of the PMOS device. (Specification, Pages 35-36, Paragraphs [00128] to [00129], Figure 34). The intrinsic base 3410 and the LDDs 3420 and 3430 each receive the same dopant because they are simultaneously doped with the same dopant process. An implant procedure is used to dope the intrinsic base 3510 of the PNP device and the LDDs 3520 and 3530 of the NMOS device. (Specification, Pages 36-37, Paragraphs [00131] to [00132], Figure 35). The intrinsic base 3510 and the LDDs 3520 and 3530 each receive the same dopant because they are simultaneously doped with the same dopant process.

A dielectric layer 3600 is deposited and anisotropically etched to form spacers on the inside of the hole for the emitters of the bipolar transistors and on the outside of the gate poly for the bipolar transistors. (Specification, Page 37, Paragraphs [00134] to [00135], Figure 36-37).

A second polysilicon layer 3800 (Poly2 3800) is then deposited and doped to form (1) an NPN emitter 3910 in the NPN device and (2) an NPN deep collector 3920 in the NPN device and (3) an NMOS source/drain 3930 in the NMOS device, and (4) a PMOS well contact 3940 in the PMOS device. (Specification, Pages 37-39, Paragraphs [00136] to [00140], Figures 38-39). The four doped portions (3910, 3920, 3930, 3940) each receive the same dopant because they are simultaneously doped with the same dopant process. The second polysilicon layer 3800 (Poly2 3800) is then doped to form (1) a PNP emitter 4010 in the PNP transistor and (2) a PNP deep collector 4020 in the PNP transistor and (3) an NMOS well contact 4030 in the NMOS transistor, and (4) a PMOS source/drain 4040 in the PMOS transistor. (Specification, Pages 39-40, Paragraphs [00141] to [00143], Figure 40). The four doped portions (4010, 4020, 4030, 4040) each receive the same dopant because they are simultaneously doped with the same dopant process.

Then portions of the second polysilicon layer 3800 (Poly2 3800) are etched to define the emitters and collectors of the NPN device and of the PNP device and to define the sources and drains of the NMOS device and of the PMOS device. (Specification, Pages 40-41, Paragraph [00144], Figures 41-43).

Support for Independent Claims **37 C.F.R. § 41.37 (c)(1)(v)**

Note that, per 37 C.F.R. § 41.37, only the independent claim (Claim 1)is discussed in this section. The discussion of the independent claim in this section is for illustrative purposes and is not intended to affect the scope of the claim.

Regarding Claim 1, a semiconductor apparatus is claimed that comprises at least one double poly bipolar transistor (PNP device, NPN device) and at least one double poly metal oxide semiconductor (MOS) transistor (PMOS device, NMOS device) in which (1) a base of the double poly bipolar transistor and (2) a gate of the double poly metal oxide semiconductor (MOS) transistor contain substantially identical dopants.

The PNP device of the invention is a double poly bipolar transistor that comprises a first layer of polysilicon 2700 and a second layer of polysilicon 3800. Similarly, the NPN device of the invention is a double poly bipolar transistor that comprises a first layer of polysilicon 2700 and a second layer of polysilicon 3800. The PMOS device of the invention is a double poly metal oxide semiconductor (MOS) transistor that comprises a first layer of polysilicon 2700 and a second layer of polysilicon 3800. Similarly, the NPN device of the invention is a double poly bipolar transistor that comprises a first layer of polysilicon 2700 and a second layer of polysilicon 3800.

The PNP device comprises an extrinsic base 2810 that contains substantially identical dopants as the NMOS gate 2820 of the NMOS device. This is because the extrinsic base 2810 and the NMOS gate 2820 were simultaneously doped with the same dopant process.

The NPN device comprises an extrinsic base 2910 that contains substantially identical dopants as the PMOS gate 2920 of the NMOS device. This is because the extrinsic base 2910 and the PMOS gate 2920 were simultaneously doped with the same dopant process.

Therefore, the elements of independent Claim 1 are fully supported.

Grounds of Rejection to be Reviewed on Appeal **37 C.F.R. § 41.37 (c)(1)(vi)**

1. Claims 1-3, 7-9, 13-17 and 21 are rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 4,902,640 to Sachitano et al. ("*Sachitano*") .

2. Claims 4, 10 and 20 are rejected under 35 U.S.C. § 103(a) as being obvious over *Sachitano* in view of United States Patent No. 6,441,441 to Suda ("*Suda*").

Argument **37 C.F.R. § 41.37 (c)(1)(vii)**

Stated Grounds of Rejection for Claims 1-4

Ground of Rejection 1: Claims 1-3, 7-9, 13-17 and 21 are rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 4,902,640 to Sachitano et al. ("*Sachitano*").

Stated Grounds of Rejection for Claims 5-7

Ground of Rejection 2: Claims 4, 10 and 20 are rejected under 35 U.S.C. § 103(a) as being obvious over *Sachitano* in view of United States Patent No. 6,441,441 to Suda ("*Suda*").

Legal Standard for Anticipation

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 4, October 2005) (*citing In re Bond*, 910 F.2d 831, 832, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)).

Legal Standard for Obviousness

During *ex parte* examinations of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie*

basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of non-obviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 USPQ 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not be based on an applicant's disclosure. MPEP § 2142.

Evidence of a motivation to combine prior art references must be clear and particular if the trap of "hindsight" is to be avoided. *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed.Cir. 1999) (Evidence of a suggestion, teaching or motivation to combine prior art references must be "clear and particular." "Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence.'"). *In re Roufett*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed.Cir. 1998) ("[R]ejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be 'an illogical and inappropriate process by which to determine patentability.'")

Analysis of Examiner's Rejections

The cited references are briefly discussed in relevant part for the appropriate rejections, and each rejection is addressed separately below.

Ground of Rejection 1: Claims 1-3, 7-9, 13-17 and 21 are rejected under 35 U.S.C. § 102(b) as being anticipated by the *Sachitano* reference.

The limitations in Claim 1 are not taught or suggested in *Sachitano*. In particular, *Sachitano* does not teach or suggest that a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants, as required by independent Claim 1.

The January 10, 2007 Office Action stated that "Regarding Claim 1, Sachitano et al. discloses a semiconductor apparatus comprising a double-poly bipolar transistor (fig. 12, 114)

and a double-poly metal oxide semiconductor (MOS) transistor (120), wherein a base of the double-poly bipolar transistor (140) and a gate of the double-poly MOS transistor (148) contain substantially identical dopants (both NPN and PNP devices are disclosed; col. 1, lines 63-66. PNP devices would inherently have an n-type base, which is substantially identical to the n-type dopant of the MOS gate (148)." (January 10, 2007 Office Action, Page 2, Line 21 to Page 3, Line 2). For the reasons set forth below, the Appellants respectfully traverse these assertions.

The January 10, 2007 Office Action relies on a principle of inherency, stating that "PNP devices would inherently have an n-type base, which is substantially identical to the n-type dopant of the MOS gate 148." The Examiner is correct that a PNP bipolar transistor does have an n-type base by definition, but the Examiner is incorrect in therefore concluding that this has anything to do with the dopant of the MOS gate 148.

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' "*In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted, emphasis added).

"In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

The Examiner has not provided any basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art, as he is required, and so the allegation of inherency cannot support the rejection.

An n-type base, as known to those of skill in the art, is simply a transistor base in which the conduction electron density exceeds the hole density. A PNP bipolar transistor does have an n-type base.

A dopant, as known to those of skill in the art, is an impurity that is added to a semiconductor to change the number of holes and electrons relative to each other, and an n-type dopant is an impurity that "donates" weakly-bonded electrons to the semiconductor. There are different n-type dopants – phosphorus and arsenic are both n-type dopants, but are not "substantially identical". Certainly an n-type base is not substantially identical an n-type dopant, as alleged by the Examiner, as these are very different things. Further, two different n-type semiconductor elements do not necessarily have substantially identical dopants, so the claimed limitation is not an inherent feature of *Sachitano*, as alleged. In fact, Appellants respectfully submit that *Sachitano* appears to suggest differentiated doping during formation. (Column 4, Line 55 to Column 5, Line 7; Column 10, Lines 31-51).

For reference purposes, the Appellants set forth below an outline of certain major steps in the manufacture of the Appellants' invention.

A. Paragraph [00112] and Figure 28 describe how the Poly 1 layer (2700) is doped to form an extrinsic base 2810 in the PNP device and an NMOS gate 2820 in the NMOS device.

B. Paragraph [00114] and Figure 29 describe how the Poly 1 layer (2700) is doped to form an extrinsic base 2910 in the NPN device and a PMOS gate 2920 in the PMOS device.

C. Paragraph [00129] and Figure 34 describe how the intrinsic base 3410 in the NPN device is doped and how the lightly doped drains (LDD) (3420, 3430) in the PMOS device are doped.

D. Paragraph [00132] and Figure 35 describe how the intrinsic base 3510 in the PNP device is doped and how the lightly doped drains (LDD) (3520, 3530) in the NMOS device are doped.

E. Paragraph [00138] and Figure 39 describe how the Poly 2 layer (3800) is doped to form (1) NPN emitter 3910 in the NPN device, and (2) NPN deep collector 3920 in the NPN device, and (3) NMOS source/drain 3930 in the NMOS device, and (4) PMOS well contact 3940 in the PMOS device.

F. Paragraph [00141] and Figure 40 describe how the Poly 2 layer (3800) is doped to form (1) PNP emitter 4010 in the PNP device, and (2) PNP deep collector 4020 in the PNP device, and (3) NMOS well contact 4030 in the NMOS device, and (4) PMOS source/drain 4040 in the PMOS device.

Now consider the structure and method disclosed in the *Sachitano* reference.

Before the first polysilicon layer 134 is deposited in Step 29, there is a first implant step (Step 25) that is carried out for the "gate threshold voltages" of the MOS devices. Then there are two implant steps (Steps 26 and 27) that are performed "to implant collector contact region 130 to an increased N+ concentration" in the NPN device (*Sachitano*, Column 8, Lines 6-12). It is noted that Step 25, Step 26 and Step 27 are performed sequentially. Then the polysilicon layer 134 is deposited. (Step 29) (*Sachitano*, Column 8, Lines 17-19).

Sachitano then states "This layer [first polysilicon layer 134] is then masked and implanted, first, to implant the polysilicon layer to N+ concentrations over the PMOS and NMOS active device regions and over the collector contact region 130 (steps 30 and 31)." (*Sachitano*, Column 8, Lines 19-22). This first implant step includes the "gate" portions of the PMOS and NMOS devices. (See Figure 4 of *Sachitano*).

Then the N+ implant mask is stripped and the substrate is again masked and the first polysilicon layer 134 is "implanted to dope the polysilicon layer overlying the NPN bipolar active region to P+ concentrations (steps 32 and 33)." (*Sachitano*, Column 8, Lines 23-26). This second implant step includes the "base" portions of the NPN device. (See Figure 4 of *Sachitano*).

The PMOS and NMOS active device regions of the *Sachitano* device are implanted to N+ concentrations using an N type dopant (e.g., arsenic, antimony, phosphorus). Table 1 in Column 12 of *Sachitano* describes the use of phosphorus as the N type dopant. The bipolar NPN device region of the *Sachitano* device is implanted to P+ concentrations using a P type dopant (e.g., boron, indium, gallium, aluminum). Table 1 in Column 12 of *Sachitano*

describes the use of boron as the P type dopant. This clearly shows that the dopants that are used by *Sachitano* are not substantially identical.

Sachitano later implants the base region 150 of the NPN transistor. "Masking and boron implant steps (steps 37 and 38) provide P-type base region 150 for the bipolar transistor in region 114 and lightly-doped P-source and drain regions 152, 154 for the PMOSFET in region 118." (*Sachitano*, Column 8, Lines 45-49). *Sachitano* described a single implant step for the base of the NPN transistor and the lightly doped source/drain regions of the PMOS transistor. However, this implantation does not affect the shielded gate regions of the MOS transistors.

For the reasons set forth above, the Appellants respectfully submit that the *Sachitano* reference does not teach or suggest that "a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants." The Appellants respectfully submit that this feature is not inherent in the *Sachitano* reference.

Accordingly, the Appellants respectfully traverse all of the anticipation rejections of Claims 1-3, 7-9, 13-17 and 21 and respectfully request the Board to order the Examiner to withdraw the § 102 rejections with respect to these claims. The Appellants respectfully request that Claims 1-3, 7-9, 13-17 and 21 be allowed.

Ground of Rejection 2: Claims 4, 10 and 20 are rejected under 35 U.S.C. § 103(a) as being obvious over the *Sachitano* reference and the *Suda* reference.

Claims 4, 10 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the *Sachitano* reference in view of the *Suda* reference. The Appellants respectfully traverse these rejections. The Appellants respectfully submit that the Patent Office has not established a *prima facie* case of obviousness with respect to Claims 4, 10 and 20 of the Appellants' invention.

The Appellants repeat and incorporate by reference all of the comments and arguments previously made in response to the Examiner's assertions that Claims 1-3, 7-9, 13-17 and 21 of the Appellants' invention are anticipated by the *Sachitano* reference.

The January 10, 2007 Office Action stated that "Sachitano et al. discloses all of the elements of the claims as discussed in paragraph 3 above, . . . " (January 10, 2007 Office Action, Page 4, Lines 20-21). For the reasons previously set forth, the Appellants respectfully traverse this assertion. The *Sachitano* reference does not disclose all of the elements of the claims that were discussed in Paragraph 3 of the January 10, 2007 Office Action.

Claims 4, 10 and 20 each require that "at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor," where the base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants. The Examiner is correct that *Sachitano* does not teach or suggest this feature, as discussed at length above. The Examiner looks to *Suda* for this teaching. The Appellants respectfully submit that the *Suda* reference does not remedy the deficiencies of the *Sachitano* reference.

Suda describes, variously, a PMOS transistor and an NPN bipolar transistor, and indicates in each case that boron is acceptable as a P-type dopant. *Suda* does not explicitly teach that these two structures contain substantially identical dopants, and certainly one could be heavily doped while the other is lightly doped.

Even if *Suda* did include such a teaching as alleged by the Examiner, there is no proper motivation to combine these references. The motivation to combine or modify must be specific to the actual teachings sought to be combined. "In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention" *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1385 (Fed. Cir. 2001) (Emphasis added). "When the references are in the same field as that of the applicant's invention, knowledge thereof is presumed. However, the test of whether it would have been obvious to select specific teachings and combine them as did the applicant must still be met by identification of some suggestion, teaching, or motivation in the prior art, arising from what the prior art would have taught a person of ordinary skill in the field of the invention." (*In re Dance*, 160 F.3d 1339, 1343 (Fed. Cir. 1998).

The Examiner's alleged motivation is not found anywhere in the art of reference, and nothing in *Sachitano* or in *Suda* indicates that they are at all concerned with operations as a surface channel device or any particular degradation effects. Nothing in the art of reference, nor in the knowledge generally available to those of skill in the art at the time of the invention,

would motivate one to make the specific combination and modification necessary to produce the claimed invention.

The Appellants respectfully submit that one of ordinary skill, having only *Sachitano* before him, would not be prospectively moved to spontaneously assume that the substantial disclosure of *Sachitano* was in need of a base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants. In fact, the Appellants respectfully submit that *Sachitano* appears to suggest differentiated doping during formation. (Column 4, Line 55 to Column, Line 7; Column 10, Lines 31-51).

In order to overcome the admitted deficiencies of *Sachitano*, the Examiner selectively culls from *Suda* the **inference** of a base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants – even though *Suda* itself does not explicitly teach that these two structures contain substantially identical dopants. The Examiner further ignores the fact that, in order to combine the references as suggested, one of ordinary skill in the art would have to completely overlook the remainder of *Suda*'s various teachings of PMOS transistor and an NPN bipolar transistor structure and formation – teachings that vary significantly from *Sachitano*'s.

The Examiner offers that "P-type gates and N-type gates were art recognized functional equivalents for forming the conductive gate of a PMOS transistor" (January 10, 2007 Office Action, Page 5, Lines 7-8) as the motivation for one of ordinary skill in the art to embark on this speculative and selective combination process. This has no bearing at all on the Appellants' use of substantially identical dopants, as claimed.

In summary, there is neither a motivation nor a suggestion in either the cited references or the knowledge of a person of ordinary skill in the art at the time of the Appellant's invention to: 1) spontaneously assume a deficiency in *Sachitano*; 2) seek out and find *Suda*; 3) ignore almost all of *Suda*'s teachings of structure and process; 4) selectively cull a single concept from *Suda* – a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants – even though *Suda* does not explicitly disclose such; and 5) substantially modify the processes and structures of *Sachitano* to incorporate this spontaneous extraction of concept from *Suda*. Furthermore, even if the references were to be so selectively combined, the combination would still not result in the Appellants' invention as recited in independent Claim 1 or dependent Claims 4, 10 and 20 of the patent application.

For the reasons set forth above, the proposed *Sachitano-Suda* combination fails to disclose, teach, or suggest the Appellants' invention as recited in Claims 4, 10 and 20. Accordingly, the Appellants respectfully request the Board to order the Examiner to withdraw the § 103 rejections of Claims 4, 10 and 20.

In the *Sachitano* reference, both the PMOS device and NMOS device are doped with an N type dopant (phosphorus). The *Sachitano* reference also uses a separate mask and a P type implant (boron) for the NPN extrinsic base. While in the case of providing only an NPN device, this mask count is mask count neutral when compared to the mask count of the Appellants' invention. This is because the *Sachitano* reference uses a single mask for the PMOS and NMOS active regions. However, in making complementary BiCMOS the *Sachitano*

method would require an additional mask for the PNP extrinsic base. In contrast, in making complementary BiCMOS the Appellants' invention would save one mask and implant procedure.

The *Sachitano* method also adds a separate intrinsic base implant. This is because it includes the PMOS PLDD in the NPN intrinsic base but adds an additional dedicated mask and implant to augment the base doping. In contrast, the Appellants' invention uses the same mask and implant to form the PLDD and the NPN intrinsic base and the NLDD and the PNP intrinsic base. In the case of complementary bipolar or complementary BiCMOS, this feature saves two masking layers and implants (and the associated cycle time and costs) over the prior art.

The complementary doping of the MOS gates in the Appellants' invention enables complementary doping of the extrinsic base and, therefore, the formation of both NPN devices and PNP devices. The complementary doping of the gates provides better threshold matching and control. For these reasons, the Appellants' invention provides significant improvements over the technology that is disclosed in the prior art.

All claim rejections are respectfully traversed. Reconsideration and allowance of Claims 1-4, 7-10, 13-17 and 20-21 are respectfully requested.

The Appellants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing arguments and response. The Appellants reserve the right to submit further arguments in support of his above stated position as well as the right to introduce relevant secondary considerations including long-felt but unresolved needs in the industry, failed attempts by others to invent the invention, and the like, should that become necessary.

The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for the allowance of Claims 1-4, 7-10, 13-17 and 20-21.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Munck Butrus Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS, P.C.

Date: June 11, 2007

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	RICHARD W. FOOTE ET AL.
Serial No.:	10/777,012
Filed:	February 11, 2004
For:	SEMICONDUCTOR APPARATUS COMPRISING BIPOLAR TRANSISTORS AND METAL OXIDE SEMICONDUCTOR TRANSISTORS AND MANUFACTURING METHOD
Group No.:	2891
Examiner:	Steven J. Fulk

APPENDIX A - Claims Appendix 37 C.F.R. § 41.37 (c)(1)(viii)

1. (Previously Presented) A semiconductor apparatus comprising at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor, wherein a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants.

2. (Previously Presented) The semiconductor apparatus as set forth in Claim 1 wherein said at least one double poly bipolar transistor and said at least one double poly metal

oxide semiconductor (MOS) transistor comprise a substrate and a first layer of polysilicon (Poly1) material wherein:

said first layer of polysilicon (Poly1) material in said at least one double poly bipolar transistor is doped with impurity ions to form an extrinsic base; and

said first layer of polysilicon (Poly1) material in said at least one double poly MOS transistor is doped with impurity ions to form an MOS transistor gate.

3. (Original) The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

4. (Original) The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

5.-6. (Cancelled)

7. (Original) The semiconductor apparatus as set forth in Claim 2 wherein:

said substrate is implanted with impurity ions to form an intrinsic base in said at least one double poly bipolar transistor; and

said substrate is simultaneously implanted with impurity ions to form a lightly doped drain in said at least one double poly MOS transistor.

8. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said lightly doped drain in said at least one double poly MOS transistor is self aligned.

9. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

10. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

11.-12. (Cancelled)

13. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor and said at least one double poly metal oxide semiconductor (MOS) transistor further comprise a second layer of polysilicon (Poly2) material wherein:

said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor is doped with impurity ions to form an emitter; and

said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor is simultaneously doped with impurity ions to form an MOS source/drain.

14. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said emitter in said at least one double poly bipolar transistor is self aligned to an extrinsic base of said at least one double poly bipolar transistor.

15. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said MOS source/drain in said at least one double poly MOS transistor is self aligned to a gate of said at least one double poly MOS transistor.

16. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor is simultaneously doped with impurity ions to form a deep collector.

17. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said MOS source/drain in said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor is etched to separate said MOS source/drain into a source and a drain.

18.-19. (Cancelled)

20. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

21. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

22. (Withdrawn) A method for manufacturing a semiconductor apparatus comprising at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor, said method comprising the steps of:

manufacturing said at least one double poly bipolar transistor in said semiconductor apparatus; and

simultaneously manufacturing said at least one double poly metal oxide semiconductor (MOS) transistor in said semiconductor apparatus.

23. (Withdrawn) The method as set forth in Claim 22 further comprising the steps of:

applying a first layer of polysilicon (Poly1) material to a substrate of said semiconductor apparatus;

doping said first layer of polysilicon (Poly1) material in said at least one double poly bipolar transistor with impurity ions to form an extrinsic base; and

simultaneously doping said first layer of polysilicon (Poly1) material in said at least one double poly MOS transistor with impurity ions to form an MOS transistor gate.

24. (Withdrawn) The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

25. (Withdrawn) The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

26. (Withdrawn) The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

27. (Withdrawn) The method as set forth in Claim 23 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

28. (Withdrawn) The method as set forth in Claim 23 further comprising the steps of:

implanting said substrate with impurity ions to form an intrinsic base in said at least one double poly bipolar transistor; and

simultaneously implanting said substrate with impurity ions to form a lightly doped drain in said at least one double poly MOS transistor.

29. (Withdrawn) The method as set forth in Claim 28 wherein said lightly doped drain in said at least one double poly MOS transistor is self aligned.

30. (Withdrawn) The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

31. (Withdrawn) The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

32. (Withdrawn) The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

33. (Withdrawn) The method as set forth in Claim 28 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

34. (Withdrawn) The method as set forth in Claim 28 further comprising the steps of:

applying a second layer of polysilicon (Poly2) material to said at least one double poly bipolar transistor and to said at least one double poly metal oxide semiconductor (MOS) transistor;

doping said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor with impurity ions to form an emitter; and

simultaneously doping said second layer of polysilicon (Poly2) material in said at least one double poly metal oxide semiconductor (MOS) transistor with impurity ions to form an MOS source/drain.

35. (Withdrawn) The method as set forth in Claim 34 wherein said emitter in said at least one double poly bipolar transistor is self aligned to an extrinsic base of said at least one double poly bipolar transistor.

36. (Withdrawn) The method as set forth in Claim 34 wherein said MOS source/drain in said at least one double poly MOS transistor is self aligned to a gate of said at least one double poly MOS transistor.

37. (Withdrawn) The method as set forth in Claim 34 further comprising the step of:

simultaneously doping said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor with impurity ions to form a deep collector.

38. (Withdrawn) The method as set forth in Claim 34 further comprising the step of:

etching said MOS source/drain in said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor to separate said MOS source/drain into a source and a drain.

39. (Withdrawn) The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

40. (Withdrawn) The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

41. (Withdrawn) The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

42. (Withdrawn) The method as set forth in Claim 34 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

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APPENDIX B
Evidence Appendix
37 C.F.R. § 41.37 (c)(1)(ix)

None

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APPENDIX C
Related Proceedings Appendix
37 C.F.R. § 41.37 (c)(1)(x)

None